PRODUCT RELIABILITY REPORT

Product: JW1756O

	Name	Position
Prepared By	Fen Shi	Quality Engineer
Checked By	Yanjun Xiang	Product Manager
Checked By	Houye Yang	QA Manager
Approved By	Frank Ren	VP of Quality

Quality Department

Joulwatt Technology (Hangzhou) CO.,LTD.

1. Device Information

Product:	JW1756O
Lot# or DateCode:	AJ36RC.1
Package:	SOP8
Report Date:	2018/4/6

2. Summary of Test Results

Test Items	Test condition	S.S.	Acc/Re	Fail/Pass	Test Result	Remark
High Temperature Operating Life	JESD22-A108, @+125°C for 1000 Hours or equivalent	77	0/1	0/77	PASS	
ESD: Human Body Model (HBM)	MIL-STD-883J Method 3015.9	18	0/1	0/18	PASS	＞3KV
Latch-up	EIA/JESD78	9	0/1	0/9	PASS	>+/-100mA & >1.5Vccmax
Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing (Precondition L3)	Bake: 125℃,24h Soak: 30℃, 60%RH , 192h Reflow: 260℃, 3times	308	0/1	0/308	PASS	MSL=3
Temperature Cycling (TCT)	JESD22-A104 -65℃-150℃, Dwell=15min,500/ 1000Cycles	77	0/1	0/77	PASS	
Accelerated Moisture Resistance-Unbiased Autoclave (PCT)	JESD22-A102 121℃ 100%RH, 205 kPa,168h	77	0/1	0/77	PASS	

Steady State Temperature Humidity Bias Life Test (THT)	85℃'85%RH, 500/1000h	77	0/1	0/77	PASS	
High Temperature Storage Life (HTSL)	JESD22-A103 Ta=150℃,500/1000h	77	0/1	0/77	PASS	

3. Failure Rate Calculation

Sample Size:	980
Rejects:	0
Activation Energy (eV):	0.7
Equivalent Device Hours:	7.638×10^{7} Hours
Failure Rate (FIT@60%CL):	4.849 FIT
MTBF (years):	23,539 Years

Appendix: Description of Reliability Test and Failure Rate Calculation

High Temperature Operating Life Test

Purpose: This test is a worst-case life test that checks the integrity of the product. The high temperature testing is use for acceleration of any potential failures over time. The calculation for failure rate (FIT) using the operating ambient temperature is done using the arrhenius equation.

Condition: 125℃ @ Vccmax

Pass Criteria: All units must pass the min/max limits of the datasheet.

ESD Test

Purpose: The purpose of the ESD test is to guarantee that the device can withstand electrostatic voltages during handling.

Condition: Human Body Model, Machine Model and Charged Device Model.

Pass Criteria: ESD Testing on every pin. The device must be fully functional after testing and pass the min/max limits in the datasheet.

IC Latch-Up Test

Purpose: The purpose of this specification is to establish a method for determining IC latch-up characteristics and to define latch-up failure criteria. Latch-up characteristics are extremely important in determining product reliability and minimizing No Trouble Found (NTF) and Electrical Overstress (EOS) failures due to latch-up.

Condition: Voltage and current injection

Pass criteria: All pins with the exception of “no connect” pins and timing related pins, shall be latch-up tested. The device must be fully functional after testing and pass the min/max limits in the datasheet.

Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing

Purpose: The purpose of this standard is to identify the classification level of nonhermetic solid state surface

mount devices (SMDs) that are sensitive to moisture-induced stress so that they can be properly packaged, stored, and handled to avoid damage during assembly solder reflow attachment and/or repair operations.

Condition: Bake + moisture sock + 3X reflow at 260℃

Pass criteria: All units must pass the min/max limits of the datasheet

Accelerated Moisture Resistance- Unbiased Autoclave

Purpose: To check the performance of the device in humid environments. This test checks the integrity of the passivation, poor metal to plastic seal and contamination level during assembly and material compatibility.

Condition: 121℃/15psig/100% RH (no bias)

Pass Criteria: All units must pass min/max limits of the datasheet.

Temperature Cycle Test

Purpose: This test is used to evaluate the die attach integrity and bond integrity. This is similar to the Thermal Shock test, but can generate different failure modes due to the longer dwell time and gradual temperature change.

Condition: -65℃ to 150℃

Pass Criteria: All units must pass min/max limits of the datasheet.

Steady State Temperature Humidity Bias Life Test

Purpose: This is to check the performance of the device in humid environments. This test checks the integrity of the passivation, poor metal to plastic seal and contamination level during assembly and material compatibility.

Condition: 85%RH at 85℃ with Vcc=Vccmax

Pass Criteria: All units must pass min/max limits of the datasheet.

High Temperature Storage Life

Purpose: This test is basically used to determine if the effects of diffusion, oxidation, intermetallic growth, and chemical degradation of packaging components will affect product life.

Condition: Ta=150℃+ Preconditioning if Required,T=1000h

Pass Criteria: All units must pass min/max limits of the datasheet.

Failure Rate Calculation

The failure rate for a technology is gauged by a Failures-In-Time (FIT) based upon accelerated stress data. The units for FIT are failures per billion device hours.

$$FITRate = \frac{(\chi^2 / 2) * 10^9}{stress * device\ hours}$$

The stress that enables FIT is High Temperature Operating Life (HTOL), which is a product level test. HTOL is accelerated by temperature and by voltage. The total number of failures in stress determines the chi-squared factor (a dimensionless number representing a 60% confidence level of statistics). The number of product units times the stress period (in hours) is the device-hours number. The Arrhenius equation uses the Activation Energy for the failure mode, as well as the stress temperature and the reporting temperature (usually 55C) to compute the HTOL temperature acceleration factor, AF(T). The accelerated stress device-hours is AF(T) times the device-hours number. For voltage stress, the voltage acceleration factor AF(V)= Exp(β(Vtest- Vuse)), Vtest = Stress Voltage (V). Vuse = Nominal Voltage (V). β = Voltage Acceleration Constant depending on a wafer process.

MTBF (Mean Time Between Failure) equals to 1/FIT.